REMARKS

The Assignee of this application (hereafter referred to as "Assignee" for convenience) respectfully asks for reconsideration of both this application and the Office Action dated October 6, 2006. A response to this Office Action was due by January 6, 2007. Accordingly, Assignee is submitting a Petition for a three month extension of time with this Amendment. The Commissioner is authorized to charge the associated Petition fee of $1020, together with any other fees that may be necessary for the entry and consideration of this Amendment and to maintain the pendency of this application, including any fees under 37 C.F.R. §1.16 or §1.17, to Deposit Account No. 19-0733. The period for responding to the outstanding Office Action is thus extended up to and through April 6, 2007. Please consider this Amendment as timely filed.

In the Office Action, the Primary Examiner rejected claims 59-72 and 74-82 under 35 U.S.C. §102(a) over the IBM Technical Disclosure.[1] Assignee respectfully traverses this rejection, and courteously asks for its reconsideration.

In making this rejection, the Primary Examiner alleged that the "IBM document discloses interconnected programmable chips on a substrate which are connected to and configured by another chip or part of a chip." (See Office Action, page 2, lines 26-28.) Assignee respectfully submits that the Primary Examiner's assertion is not entirely correct. As illustrated in Figure 1, the chips 2 are connected by wiring line segments 3 formed on a "silicon wiring wafer 1...used as a carrier for chips 2 and as a chip interconnection means." (See the IBM Technical Disclosure,

1 It is Assignee's understanding that the Examiner is referring to the IBM Technical Disclosure entitled "Logically Controlled Chip Interconnection Technique."

lines 1 and 2.) Thus, the IBM Technical Disclosure appears to teach something akin to a configurable printed circuit board, not an interconnect chip. Contrary to the Primary Examiner's suggestion, nothing in the IBM Technical Disclosure would teach or suggest that a chip 2 (or part of a chip 2) mounted on the wafer 1 interconnects any other chips 2 together. At most, the IBM Technical Disclosure teaches that a chip 2 could be used to control the interconnection function of the wafer 1.

Claims 59-66 and 74-76 recite

> ...at least one programmable integrated circuit mounted on the at least one second region and containing a plurality of conductive leads, the at least one programmable integrated circuit being programmable by a user to at least partially form an interconnect of selected electrically conductive traces on the printed circuit board to achieve a desired electrical function from the electronic components...

Similarly, claims 67-70 and 77-79 recite

> ...at least one programmable integrated circuit chip mounted on the printed circuit board, selected ones of the second electrical contacts receiving leads from the at least one programmable integrated circuit chip thereby to enable a user to programmably at least partially form an interconnect of selected ones of the first electrical contacts so as to configure the electronic components to be mounted on the printed circuit board into a selected electrical circuit...

while claims 71, 72, and 80-82 then recite

> ...one or more programmable interconnect chips mounted on the printed circuit board, selected ones of the PIC holes receiving leads from the one or more programmable interconnect chips to enable a user to programmably at least partially form an interconnect of the electronic components into a desired electrical circuit...

Accordingly, Assignee respectfully submits that the IBM Technical Disclosure would not teach or suggest these features of the invention recited in claims 59-72 and 74-82. Assignee

instead points out that the IBM Technical Disclosure would, in fact, teach away from these features of the invention. Assignee therefore asks that the rejection of claims 59-72 and 74-82 over the IBM Technical Disclosure be withdrawn.

Next, the Primary Examiner rejected claims 59-72 and 74-82 over U.S. Patent No. 4,706,216 to Carter. Assignee respectfully traverses this rejection, and courteously asks for its reconsideration as well.

The Carter patent is directed to a configurable logic element. The Carter patent does not, however, teach or suggest using this element to interconnect a plurality of electrically conductive traces formed on a printed circuit board, as recited in 59-72 and 74-82. Instead, to the extent that the logic element of the Carter patent might be used with a printed circuit board,[2] the purpose of the Carter logic element would seem to be to insert some type of logical operation (e.g., an AND operation, an OR operation, a NOR operation, etc.) between electrically conductive traces, rather than simply connecting them as recited in claims 59-72 and 74-82.

Assignee therefore submits that the Carter patent would not teach or suggest the features of the invention recited in any of claims 59-72 and 74-82. It is thus requested that the rejection of these claims based upon the Carter patent be withdrawn.

The Primary Examiner then rejected claims 59-72 and 74-82 under 35 U.S.C. §102(e) over U.S. Patent No. 4,807,183 to Kung et al. Assignee respectfully traverses this rejection, and asks for its withdrawal as well.

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2 Assignee respectfully points out that the Carter patent does not, in fact, appear to even mention a printed circuit board.

Like the IBM Technical Disclosure and the Carter patent, the Kung et al. patent does not teach or suggest the features of the invention recited in any of claims 59-72 and 74-82. For example, claims 59-66 and 74-76 recite

> ...wherein each at least a plurality of the conductive leads is are electrically connected to a corresponding one of the electrically conductive traces formed on the printed circuit board to form an electrically conductive path from each of the component contacts to the corresponding conductive lead of the at least one programmable integrated circuit...

Claims 67-70 and 77-79 then recite

> ...at least one programmable integrated circuit chip mounted on the printed circuit board, selected ones of the second electrical contacts receiving leads from the at least one programmable integrated circuit chip thereby to enable a user to programmably form an electrically conductive interconnect path between selected ones of the first electrical contacts so as to configure the electronic components to be mounted on the printed circuit board into a selected electrical circuit...

Claims 71, 72, and 80-82 similarly recite

> ...one or more programmable interconnect chips mounted on the printed circuit board, selected ones of the PIC holes receiving leads from the one or more programmable interconnect chips to enable a user to programmably at least partially form an interconnect of the electronic components into a desired electrical circuit...

These features of the claimed invention are not taught or suggested by the Kung et al. patent.

More particularly, the Kung et al. patent does not teach or suggest forming electrically conductive paths between different contacts, as expressly recited in 59-66 and 74-76 and claims 67-70 and 77-79. For example, the device disclosed in the Kung et al. patent inserts programmable first-in, first-out (FIFO)/programmable delay (PD) circuits and pipeline register file (PRF) circuits between its inputs and outputs. (See, e.g., Figure 2 of the Kung et al. patent.)

This distinction between the device in the Kung et al. patent and the claimed invention is clearly evidenced by the fact that the direction of data travel in the Kung et al. device is one-way, from the input pins to the output pins. (See, e.g., Figure 1 of the Kung et al. patent.)

As recited in claims 59-66 and 74-76, and claims 67-70 and 77-79, however, the claimed invention provides electrically conductive paths between contacts. As would be recognized by those of ordinary skill in the art, these electrically conductive paths between contacts allows data or other signals to travel in both directions between connected electrical components. With regard to claims 71, 72, and 80-82, these claims specifically recite the presence of programmable interconnect chips (PICs). As discussed in the specification, a programmable interconnect chip according to the invention inherently provides electrically conductive paths between contacts it is configured to connect.

Assignee therefore submits that the Kung et al. patent does not teach or suggest the features of the invention recited in any of claims 59-72 and 74-82. Assignee therefore asks that the rejection of these claims over the Kung et al. patent also be withdrawn.

Finally, claims 59-72 and 74-82 were rejected under 35 U.S.C. §102(f), §102(g), and §103(a). While the Primary Examiner has stated that these rejections are "based upon the terminal disclaimer as well as the close parallelism between the instant set of claims and claims 4-8 of the '069 patent," Assignee understands that these rejections are actually predicated upon admissions made by Assignee in the Response filed on March 31, 2006. It is well-established that a terminal disclaimer serves to overcome a rejection of an Assignee's claims based upon "close parallelism" with claims in a parent patent, and cannot serve as a further basis for rejecting those

claims.

With regard to the admissions made in the Response filed on March 31, 2006, Assignee first points out that it has complied with its duty of disclosure under 37 C.F.R. §1.56. As stated in the Response filed on March 31, 2006, "[t]o the extent Assignee was able to locate the references cited by Quickturn in the above excerpt [i.e., the summary Assignee provided of Quickturn's Post-Markman invalidity allegations], copies of these are being submitted with an IDS being filed herewith." As explained in detail in that Response, the cited references that were not submitted to the Examiner were either practically or legally unavailable to the Assignee. Assignee points out that it cannot be required under 37 C.F.R. §1.56 to submit documents it cannot obtain.

While Assignee regrets its inability to provide the Examiner with each of the items listed in Quickturn's Post-Markman invalidity allegations, the Primary Examiner cannot continue to reject the pending claims based only upon those allegations without some support in the prior art. While Assignee has voluntarily relayed these allegations to the Primary Examiner, they are no different than similar allegations that might be provided directly to the Primary Examiner by an anonymous third party. Without supporting documentation that would allow the Primary Examiner to fairly judge the merits of the allegations, the Primary Examiner cannot use such allegations to reject the claims of this application. Assignee points out that it has no way to effectively rebut Quickturn's allegations during the prosecution of this application. Further, to the extent that Quickturn's allegations might have any merit, the public will be placed on notice of these allegations by the prosecution history of this application. Accordingly, Assignee again

respectfully requests that the rejections based upon the admissions made in the Response filed on March 31, 2006, be withdrawn.

In view of the above amendments and remarks, Assignee courteously urges that all of the claims are allowable, and that this application therefore is in condition for allowance. Favorable action in that regard is respectfully requested at the Primary Examiner's earliest convenience.

Respectfully submitted,

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